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JCE72 U.S. PTO  
09/887913



Class	Subclass
ISSUE CLASSIFICATION	



PATENT NUMBER
1

# U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED <i>Ede</i> Q.A. <i>TM</i>	

APPLICATION NO. 09/887913	CONT/PRIOR	CLASS <i>714</i>	SUBCLASS 718	ART UNIT <i>2183</i>	EXAMINER <i>Lamane</i>
APPLICANTS Jeffrey Lukanc					
TITLE Test bus architecture for embedded RAM and method of operating same					

PTO-2040  
12/99

ISSUING CLASSIFICATION									
ORIGINAL			CROSS REFERENCE(S)						
CLASS	SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
INTERNATIONAL CLASSIFICATION									

☐ Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.  <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	_____ (Assistant Examiner) _____ (Date)  _____ (Primary Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) _____ (Date)			ISSUE FEE	
				Amount Due	Date Paid
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